Sapphire NP™ —
Ultimately scalable, completely re-configurable test platform
A New Benchmark in ATE
Redefining Cost of Test

Economic pressures
IDMs, foundries and fabless semiconductor companies as well as assembly and test subcontractors are loudly demanding a dramatic change in test. Markets are rapidly evolving. Product innovation is accelerating in communications, information processing, gaming, video, wireless and in the high performance buses that support them. While product life cycles are shrinking, unpredictable market demands and unrelenting cost pressures abound.

The industry is changing too: ASPs are dwindling and margins eroding. On the technical front, escalating IC performance, increasing design complexity, embedded IP requiring multiple test strategies as well as new defect types and models challenge traditional test methodologies.

It’s time for a change - a revolutionary change.

Disruptive technology at work
The answer is Sapphire NP, the groundbreaking, single-platform ATE that sets new standards for performance, flexibil-
ity, cost-effectiveness and user-friendliness that reduces time-consuming test program generation. Engineered from every perspective to reduce test cost, Sapphire NP is built on the 4-D Scalable™ NPower™ architecture that enables unlimited re-configurability and truly scalable performance from DC to multi-gigahertz mixed signal test. Users define their own unique test needs and roadmaps. Featuring state-of-the-art XTOS™ software, Sapphire NP leverages industry standards in a PC-Windows environment with strong links to EDA and powerful GUI tools.

Modular architecture – scalable performance
The NPower architecture is the innovative foundation of true ATE scalability from high performance design charac-
terization to low cost production test. First and foremost, it separates platform infrastructure from performance features. The NPower architecture combines a lean Tester-per-Instrument™ framework with the patentedIsochronous Fabric Interface™ bus architecture for fast, flexible communications, a wide performance envelope and precisely synchronized plug-and-play capabilities.

The Tester-per-Instrument framework is the key to NPower platform performance flexibility. Each test instru-
ment – digital or analog – is fully encapsulated with all test resources on-board, including timing, power and memory. Complete with self-test and diagnostic capabilities, each instrument acts as an independent tester when inserted into the test head. This powerful design construct combines with the NPower universal slot architecture to

- Compact system footprint with scalable performance, from DFT to multi-gigahertz
- Unprecedented benchmark in cost-effectiveness
- Modular architecture that maximizes capital flexibility
- Field re-configurable, high-throughput digital and mixed signal instrumentation adapts to changing requirements
- Designed-in advanced DFT capabilities
- Windows-based multi-threaded software for parallel and concurrent test strategies
- Cost-effective multi-channel mixed signal instrumentation for multi-site testing
- High resolution, high accuracy Tester-per-Instrument architecture
- World-class performance Device Power Supplies ranging from 6-A to 300-A
- Architected to provide maximum throughput in multi-site testing.
Tough competition, soaring costs, faster design cycles, rising design complexity demand a revolution in Test.

The NPTest answer . . . Sapphire NP.

provide true configuration independence and eliminates the need for traditional, proprietary, expensive backplanes. Any test instrument can be plugged into any test head slot.

Linking and synchronizing the individual instruments, the high-speed Isochronous Fabric Interface bus provides lightning fast program load, data collection and communications. Its high-accuracy clock distribution guarantees edge-placement accuracy, synchronization and the performance roadmap. Native triggering-per-instrument and simplified instrument interconnect radically ease the implementation of multi-site and multi-thread test methodologies.

4-D Scalable range for long term utilization

By untying performance features from system infrastructure, Sapphire NP takes test capabilities to a 4-D Scalable dimension.

- **Performance** – Digital instruments range from DC to multi-gigahertz. Dynamically-configurable, multi-channel analog options cover 24-bit audio to 14-bit broadband video.
- **Pin count** – Without backplanes, conventional pin count limits no longer apply. The Sapphire NP universal slot framework accommodates reduced-pin or high-pin count test strategies.
- **Power** – Even the device power supplies provide high flexibility. Multiple channels on a single instrument provide the parallel test capability required for multi-site test and can be ganged to provide the high currents required for structural test of larger SOCs.
- **Price/Performance** – Sapphire NP eliminates expensive, unused performance. No more buying the highest test system performance on all pins, just to accommodate the needs of a few. With Sapphire NP configuration flexibility, users purchase specifically the combination of performance levels they need – an extraordinary reduction in Cost of Test.

Unleash the power of DFT

As companies move to incorporate more structural test to capture today’s manufacturing defects and reduce test engineering effort, Sapphire NP leverages NPTest innovation in producing the first commercially-available, exclusively structural test platform, DeFT™. Now the advantages of efficient and flexible use of scan memory, reduced pin count test methodology, enhanced DUT power management and accurate low-jitter clocks are applied to Sapphire NP.

**XTOS software, simply easy-to-use**

PC and Windows-based, XTOS applies the latest software technologies to set a new standard for high-productivity GUI tools in an ATE environment. It uses the STIL-1999 standard to bridge the gap between EDA and ATE, bringing IC design and test closer than ever before. Java-based test templates and XML test blocks provide a unique level of test program independence from the underlying operating system and form the basis of a truly extendable, plug-and-play software architecture.
EDA links through STIL
All ATE test programs rely on the use of large pattern files to represent test vectors. Traditionally these have been implemented in proprietary ASCII or even binary formats that require processor-intensive and error-prone translation when importing data from EDA tools. Once pattern debug has started in the ATE hardware, it may be impossible to take any modifications back to the original design data. The use of STIL-1999 for the test patterns in XTOS allows for direct import of the vectors generated by industry-standard EDA tools. After test patterns have been debugged using XTOS interactive GUI tools, a back-annotation path closes the loop between design and test to shorten development time and optimize yields. STIL allows for syntax extensions, so that a test system using XTOS software can apply structural, functional, mixed-signal or APG test techniques with equal proficiency.

Interactive GUI tools
XTOS offers a range of context-sensitive and interactive GUI tools for fast and efficient test program debug. The Block Editor provides a compilation-free path to test program debug, utilizing XML block structures for test data that are portable and easily extendable. Block Editor, Waveform Display and Pattern Display are interactively linked through the Test Tool Multiple Document Interface (MDI) so that test failures can quickly be compared with the related timing, levels or pattern data.

Java, XML for plug-and-play extensions
Users have different sets of needs and may want to apply unique test methodologies to their own class of devices. Recognizing this, XTOS provides Java-based test templates for all the standard methods used in DC, functional and mixed-signal testing. These Java templates can be modified and debugged by the user to create libraries of custom test methods. These validated libraries can then be efficiently deployed across a broad range of test applications by multiple test engineers. Java provides a unique advantage for this application: it offers dynamic runtime binding, which makes the test methods independent of changes to the XTOS software release.

XTOS has been designed to grow with the needs of its users. The use of XML and STIL allows for plug-and-play extensions to be added to the core software without impacting existing test templates. A Common Access Port (CAP) within XTOS allows for tester control using GUIs, user code or Python scripts, so that XTOS can adapt to provide the interactivity and flexibility required for design debug or the high-throughput and yield-optimization required for production test.

Platform for decades to come
Sapphire NP makes obsolescence obsolete. Its configuration flexibility means the system you buy today has just the functionality – analog and/or digital performance, pin count, power – you need. And with the insertion of different instruments when you need them, it’s still the ATE you’ll count on next month, next year or next decade. With unsurpassed integration providing a low cost, reliable, power-efficient infrastructure, Sapphire NP delivers on the promise of a single platform for engineering and production, in support of structural and functional test strategies at wafer sort and final test. It is a revolution in cost of ownership.